Investigation of Modulation Strategy for Cascaded H-bridge Multi level inverter fed Induction Motor Drive

Ravi kumar Bhukya[1] P. Satish kumar[2]

Abstract-In this paper a new SPWM technique using a trapezoidal triangular multicarrier space vector PWM for a 11 level cascaded H bridge multilevel inverter is simulated and compared with other types of carrier based PWM technique for performance evaluation. Different triangular carrier modulation techniques such as constant switching frequency level shift (LS) PWM technique viz, phase disposition (PD), phase opposition disposition (POD), alternative phase disposition (APOD), clamping space vector carrier based (CSVPWM), and weighted function based space vector carrier (WCSVPWM) are compared with proposed technique for symmetric structure of cascaded H bridge MLI. Simulation for 11 level CHB inverter has been carried out in MATLAB/Simulink and simulation results for voltage waveform and harmonic spectrum are presented and compared. The variation of THD with modulation index and frequency modulation for output voltages are analyzed.

Keywords-11-level cascaded inverter, CSV-PDPWM, CSV-PODPWM, CSV-APODPWM, CSV-PSPWM, TTMC-SVPDPWM, TTMC-SVPODPWM, TTMC-SVAPODPWM, TTMC-PSSVPWM, Induction motor drives, THD.

I. Introduction

Multilevel inverter (MLI) offers several advantages that make it preferable over the conventional voltage source inverter (VSI). These include the capability to handle higher DC link voltage, reduced power device stress and improved harmonics performance [1]. By using a multilevel structure, the stress on each switching device can be reduced in proportional to the higher voltages. In some applications, it is possible to avoid expensive and bulky step-up transformer [2]. Another significant advantage of a multilevel output is better and more sinusoidal voltage waveform as well as lowers THD [3]. Further, high dv/dt of semiconductor devices increases the electromagnetic interference (EMI) problem, resulting more common mode voltage and hence the stresses on the motor bearings are increased leads to possibilities of failure of motor. Thus by increasing the number of levels in the output waveform, the switching dv/dt stress is reduced in the multilevel inverter [4].

Multilevel inverters have achieved increasing acceptance in high power and high performance applications. Recently, multilevel inverters are widely used as static var compensators, active power filters and in motor drive applications. The advantages of multilevel inverters are good power quality, low switching loss and high voltage capability [5].

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The topologies of multilevel inverters are classified into three types: flying capacitor, diode clamped and cascaded multilevel inverters [6].

The cascaded H-bridge (CHB) multilevel inverter (MLI) is widely used due to the modularity and simplicity of the control. A single-phase five level cascaded multilevel inverter is contain Each dc source connected with its H-bridge generates three different output voltages, $+Vdc$, 0, and Vdc using various combinations of switching with the 4 switches. With two symmetric H-bridges in cascade, five level $+2Vdc$, $+Vdc$, 0, $-Vdc$, $-2Vdc$ of output voltage can be produced. The overall output voltage of CHB MLI is given by: $Vo1 = Vdc1 + Vdc2 + ... + Vdcn$.

In this paper, constant low switching frequency based on carrier pulse width modulation methods are presented and compared. A new modulation method called trapezoidal triangular multi carrier space vector PWM (TTMC-SVPWM) SPWM is implemented and compared with other methods. This new modulation method gives advantages in multilevel inverter to minimize the percentage of total harmonic distortion (THD) and to increase the output voltage.

II. Multi Carrier Based PWM Techniques

By implementing modulation technique, low frequency voltage harmonics are removed perfectly. This modulation technique produces nearly perfect sinusoidal wave forms, with lower THD.A very wide spread method in industrial applications is the classic carrier-based Si-up to $2N_{th}$ carrier group, where N_c is the number of H-bridges in each phase. Phase Shifted Carrier PWM (PSCPWM) is the common PWM for cascaded MLI. The switching transitions for PSCPWM are 2N times the number of switching transitions for APOD. The vertically shifted carrier scheme can be easily realizable on any digital controller. This scheme comes with three different techniques:

- All carrier signals are in phase (Phase Dispositions (PD)).
- In which each carrier is phase shifted by 1800 from its neighboring carrier(Alternative Phase Opposition Dispositions (APOD)).
- All carriers above the sinusoidal reference zero point are $180\circ$ out of phase with those bellow the reference zero point (Phase Opposition Dispositions (POD))

In the APOD, the sideband harmonics corresponding to first set are centered around the carrier frequency. In the APOD and the POD, harmonics will not exist at pulse number mf, due to odd symmetry of their PWM waveforms [7]. The APOD and the POD strategies provide similar performance for three level converters [8]. In PD, the triplen harmonics of voltage will be removed because the waveforms are asymmetric and thus harmonics at mf are removed if mf is chosen as a multiple of three. So the PD is more expedient due to minute values of other harmonics. The PD strategy is now well recognized for attaining the lowest line-to-line harmonic voltage distortion [9].

A. Modulation index

The modulation index is the ratio of peak magnitudes of the modulating signal V_m and the carrier signal:

$$m = \frac{Vm}{Vc} \tag{1}$$

The modulation index in SPWM technique for cascaded multilevel inverter configuration is given by:

$$m = \frac{Vm}{(N-1)Vc} \tag{2}$$

where N is number of levels. For under modulation $0 < m < 1$. For over modulation $m > 1$.

Generally, over modulation is not desired because of the presence of the lower frequency harmonics in the output voltage and subsequent distortion in the load current.

B. Frequency modulation

It is the ratio of frequency of the triangular carrier signal f_c to the frequency of sinusoidal reference signal f_s. It controls harmonics in the output voltage.

$$mf = \frac{f_c}{f_s} \tag{3}$$

III. Generaltized TTMC-SPACE Vector PWM For Cascaded Multi Level Inverter

This paper presents a modified Space vector Pulse width modulation technique so called Clamping Space vector Pulse width modulation(CSV-PWM) technique, In this paper the reference sine wave generated as in case of conventional off set injected SVPWM technique is modified by down sampling the reference wave by order of 10. Thus the waveform will be discretised reference modified Sine wave which when compared with the carrier techniques such as PD, POD, APOD and PS will generated the accurate PWM pulses for the proposed cascaded multi-level inverter. The problem DC bus unbalance has suppressed to maximum extent. And this paper presents weighted clamping Space vector Pulse width modulation(WCSV-PWM) technique, in this techniques gives the some weight function down sampling the reference waves. Thus the waveform will be discretised reference modified Sine wave which when compared with the carrier techniques such as PD, POD, APOD and PS will generated the accurate PWM pulses for the proposed cascaded multi-level inverter.

The modified SVPWM method offers a good opportunity for the realization of the Three-phase inverter control. In case of the eleven level inverters it is better to use the modified SVPWM method and with three reference waves compared to PD, POD, APOD and PS-PWM carrier waves with each phase . In such case the motor harmonic losses will be considerably lower [10].In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [11]. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, T_{offset}, is added to the reference phase voltages. where the magnitude of T_{offset} is given by,

$$T_{offset} = \frac{-(T_max + T_min)}{2} \tag{4}$$

In this paper, a simple technique to determine the offset voltage (To be added to the reference phase voltage for PWM generation

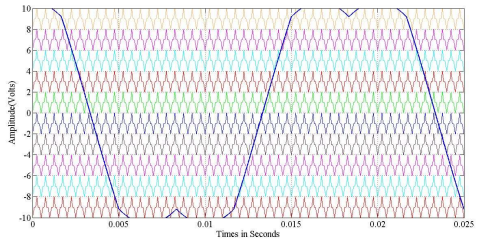

Fig. 1: TTMC-PDSVPWM

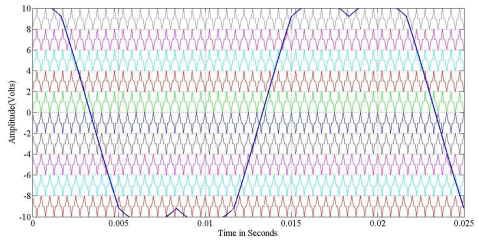

Fig. 2: TTMC-PDSVPWM

for the entire modulation range) is presented, based onely on the sampled amplitudes of the reference phase voltages [12]. The proposed modified reference PWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, the procedure for this is given in [13]. An offset time, offset T , is added to the reference phase voltages where the magnitude of T_{offset} given by,

$$T_a = \frac{-(V_a * T_s)}{Vdc} \tag{5}$$

$$T_b = \frac{-(V_b * T_s)}{Vdc} \tag{6}$$

$$T_c = \frac{-(V_c * T_s)}{Vdc} \tag{7}$$

T_a, T_b and T_c are the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages.

$$T_{offeset} = [\frac{T_o}{2} - T_{min}] \tag{8}$$

$$T_o = [T_s - T_{offeset}] \tag{9}$$

$$T_{offeset} = [T_{max} - Tmin] \tag{10}$$

The pulse generation of the different carried based SVPWM techniques shown in bellows figures. Fig. 1: Indicates the TTMC-PDSVPWM techniques, Fig. 2: Indicates the TTMC-PODSVPWM techniques, Fig. 3: Indicates the TTMC-APODSVPWM techniques, Fig. 4: Indicates the PD-SVPWM techniques, Fig. 5: Indicates the CSV-PDPWM techniques and Fig. 6: Indicates the weighted CSV-PDPWM techniques,

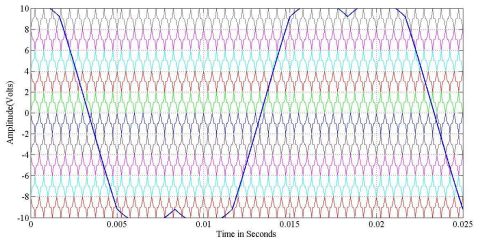

Fig. 3: TTMC-APODSVPWM

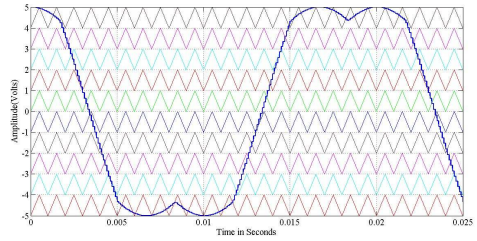

Fig. 4: PD-SVPWM

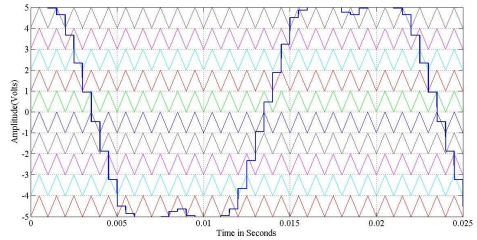

Fig. 5: CSV-PDPWM

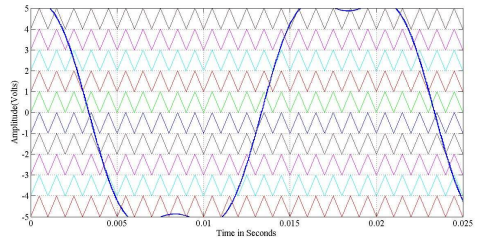

Fig. 6: CSV-PDPWM

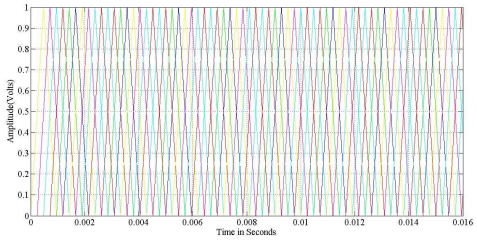

Fig. 7: CSV-PDPWM

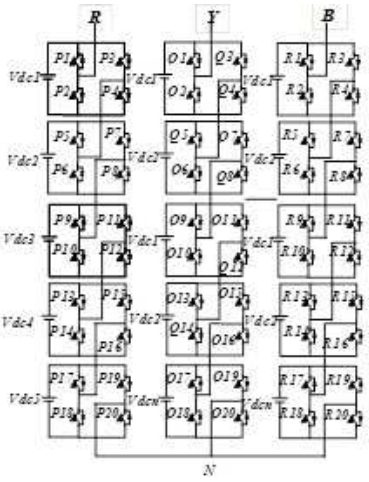

Fig. 8: 11-Level cascaded H-bridge inverter

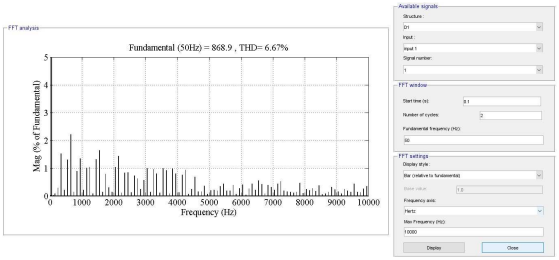

Fig. 9: PD-SPWM

IV. Simulation Results And Discussion

The simulation of cascaded H-bridge multi-level inverter with proposed comparison of control strategies applied to three phase eleven level cascaded multi-level inverter is simulated by MATLAB/SIMULINK. The output line voltages are of $398V$ magnitude peak to peak as for the DC input of $400V$. The number level in phase voltage is $2N_c + 1$, where Nc is number of single phase inverter cells used in a phase and the number of level in line voltage is $2m - 1$, where m is the number of levels in phase voltage. CMLI researches the higher output voltage and power levels. Fig. 8.Showns 11-level cascaded H-bridge inverter.

Fig. 9, Fig. 10, Fig. 11 and Fig. 12 show the harmonic analysis of inverter output line voltage for dierent SPWM techniques with the triangular carrier wave having mf of 21. The fundamental component of output voltage in all the PWM techniques is almost the same but 15% more than all the SPWM techniques. The performance of PODPWM and APODPWM techniques is almost the same in terms of THD. The PDPWM technique gives 6.67% of THD, which gives better performance with respect to all other techniques. If the carrier frequency increases, the THD in PDPWM, PODPWM,APODPWM and PSPWM techniques reduces, whereas no change is observed in

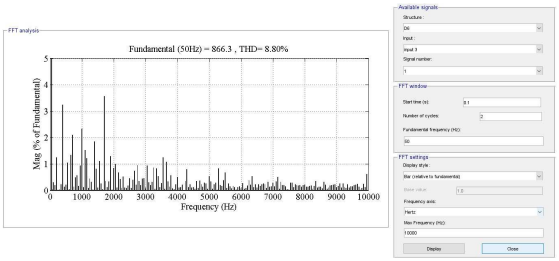

Fig. 10: POD-SPWM

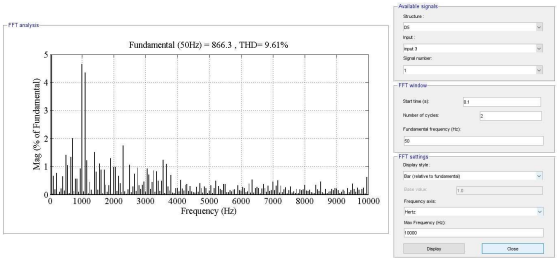

Fig. 11: APOD-SPWM

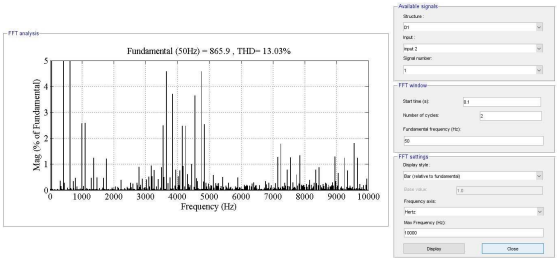

Fig. 12: PS-SPWM

the magnitude of fundamental component.

Fig. 13, Fig. 14, Fig. 15 and Fig. 16 show the harmonic analysis of inverter output line voltage for dierent modified SVPWM techniques with the triangular carrier wave having mf of 21. The fundamental component of output voltage in all the PWM techniques is almost the same but 15% more than all the SPWM techniques. The performance of PODSVPWM and APODSVPWM techniques is almost the same in terms of THD. The PDSVPWM technique gives 5.35% of THD, which gives better performance with respect to all other techniques. If the carrier frequency increases, the THD in PDSVPWM, PODSVPWM,APODSVPWM and PSSVPWM techniques reduces, whereas no change is observed in the magnitude of fundamental component.

Fig. 17, Fig. 18, Fig. 19 and Fig. 20 show the harmonic analysis of inverter output line voltage for dierent CSVPWM techniques with the triangular carrier wave having mf of 21. The fundamental component

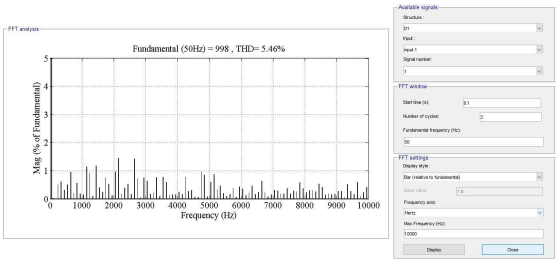

Fig. 13: PD-SVPWM

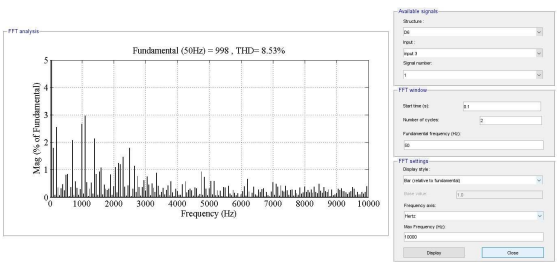

Fig. 14: POD-SVPWM

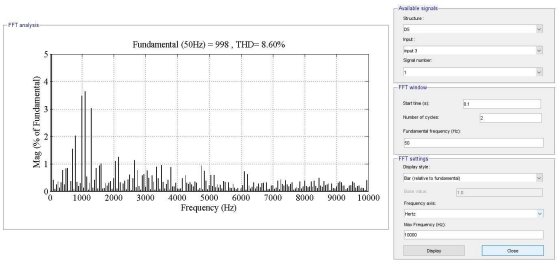

Fig. 15: APOD-SVPWM

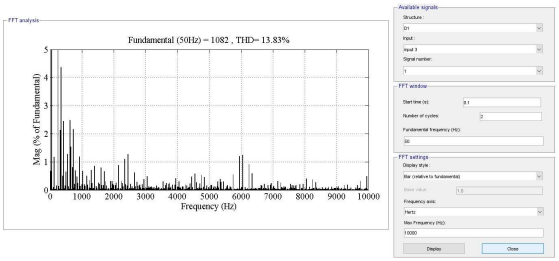

Fig. 16: PS-SVPWM

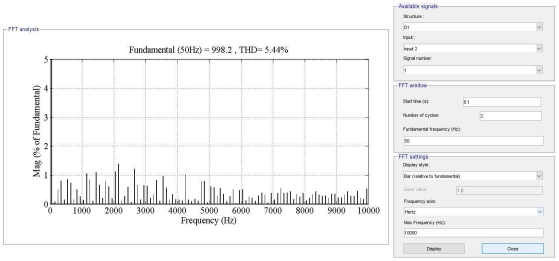

Fig. 17: CSV-PDPWM

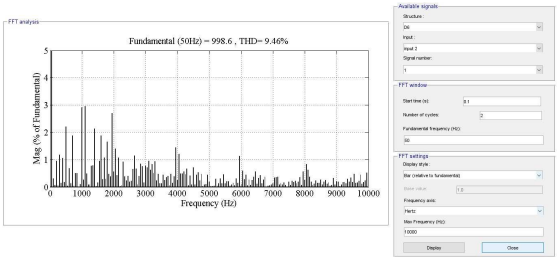

Fig. 18: CSV-PODPWM

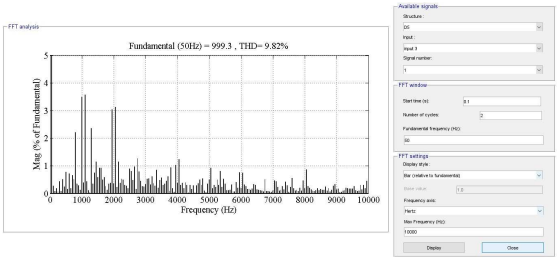

Fig. 19: CSV-APODPWM

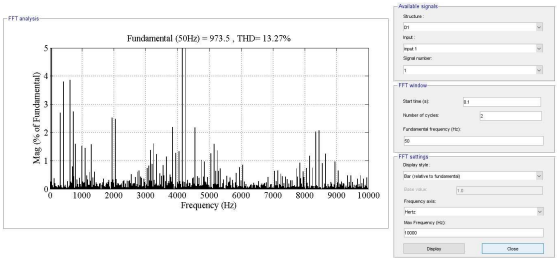

Fig. 20: CSV-PSPWM

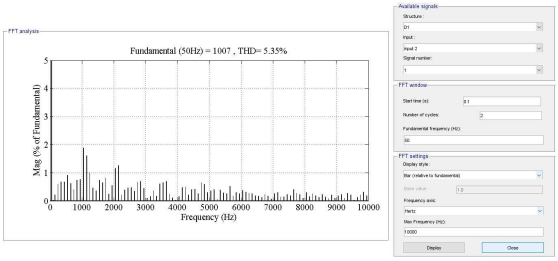

Fig. 21: WCSV-PDPWM

of output voltage in all the PWM techniques is almost the same but 15% more than all the SPWM techniques. The performance of CSVPODSVPWM and CSVAPODSVPWM techniques is almost the same in terms of THD. The CSVPDSVPWM technique gives 6.77% of THD, which gives better performance with respect to all other techniques. If the carrier frequency increases, the THD in CSVPDSVPWM, PODSVPWM APODSVPWM and PSSVPWM techniques reduces, whereas no change is observed in the magnitude of fundamental component.

Fig. 21, Fig. 22, Fig. 23 and Fig. 24 show the harmonic analysis of inverter output line voltage for dierent weighted function of CSVPWM techniques with the triangular carrier wave having mf of 21. The fundamental component of output voltage in all the PWM techniques is almost the same but 15% more than all the SPWM techniques. The performance of PODSVPWM and APODSVPWM techniques is almost the same in terms of THD. The PDSVPWM technique gives 5.35% of THD, which gives better performance with

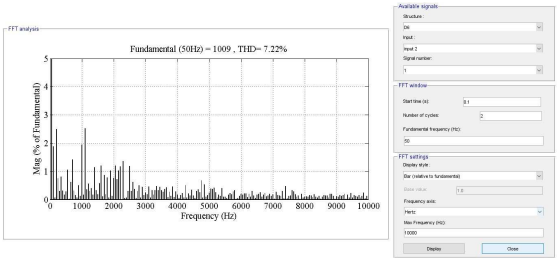

Fig. 22: TTMC-PDSVPWM

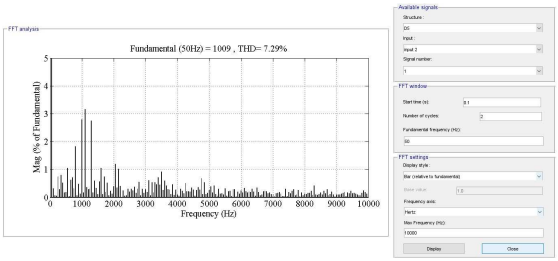

Fig. 23: WCSV-APODPWM

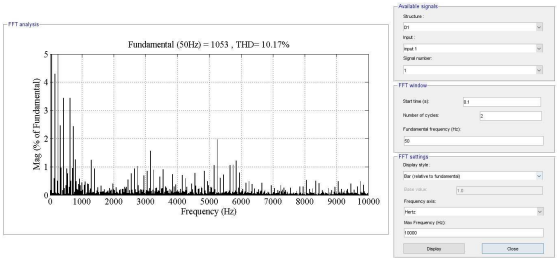

Fig. 24: WCSV-PSPWM

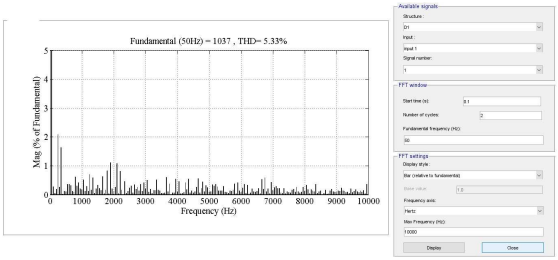

Fig. 25: TTMC-PDSVPWM

respect to all other techniques. If the carrier frequency increases, the THD in WPDSVPWM, PODSVPWM,APODSVPWM and PSSVPWM techniques reduces.

Fig. 25, Fig. 26, Fig. 27 and Fig. 28 show the harmonic analysis of inverter output line voltage for dierent modified trapezoidal triangular carrier based TTMC-SVPWM techniques with the triangular carrier wave having mf of 21. The fundamental component of output voltage in all the PWM techniques is almost the same but 15% more than all the SPWM techniques. The performance of TTMC-PDSVPWM and TTMC-PODSVPWM techniques is almost the same in terms of THD. The TTMC-PDSVPWM technique gives 5.35% of THD, which gives better performance with respect to all other techniques. If the carrier frequency increases, the THD in TTMC-PDSVPWM, TTMC-PODSVPWM TTMC-APODSVPWM and TTMC-PSSVPWM techniques reduces, whereas no change is observed in the magnitude of fundamental component.

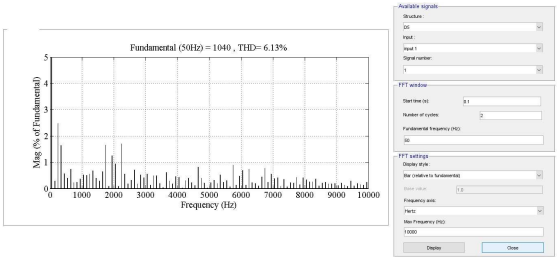

Fig. 26: TTMC-PODSVPWM

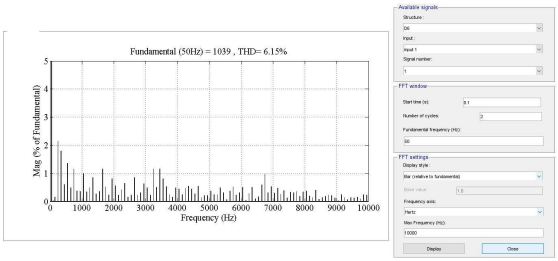

Fig. 27: TTMC-APODSVPWM

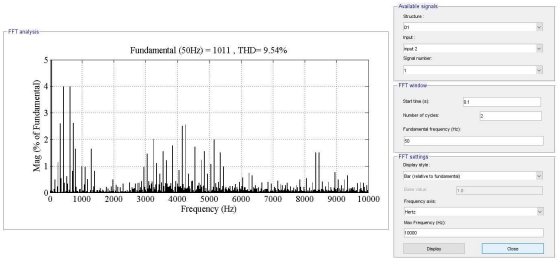

Fig. 28: TTMC-PSSVPWM

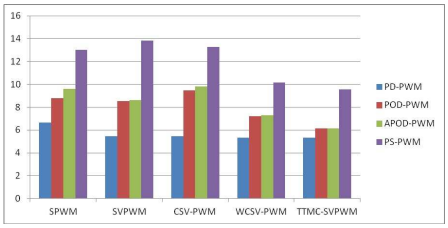

Fig. 29: THD comparison for different modulation strategy

The eleven level CMLI was simulated with induction motor load, and the DC voltage given is $100V$. In the eleven level single phase CMLI contain five H-bridges with series connections with the output phase voltage is 11 level and line voltage is 21 level of the inverter. Fig. 1. shows the circuit arrangement for 11-level CMLI with PWM generator. With perfect voltage and current shapes of the eleven level CMLI. The comparison of total harmonic distroction of different modulation strategy SPWM, modified SVPWM, clamping based CSV-PWM, weighted function based CSV-PWM and trapezoidal triangular carrier based TTMC-SVPWM techniques. In PSCPWM techniques for all different modulation strategy the harmonics are shifted towards higher frequency and compared the THD for different modulation techniques show in bellow graph (Fig. 29).

V. Conclusion

This paper present simulation results for a Eleven level cascaded H bridge inverter in symmetric configuration using various types of PWM like level shift constant switching frequency (PD, POD, APOD) PWM, phase shift PWM, modified SVPWM, clamping space vector based PWM (CSVPWM), weighted function based space vector PWM (WCSVPWM) and trapezoidal triangular carrier based space vector PWM (TTMC-SVPWM) techniques. The based on simulation results are compared. The proposed trapezoidal triangular carrier space vector PWM wave as new multi carrier for sinusoidal pulse width modulation technique gave minimum THD of 5.33%, whereas corresponding values are high in triangular LS- PWM, PSC-PWM, CSV-PWM, and WCSV-PWM for the symmetrical structure. The output voltage with the proposed TTMC SVPWM is also second highest, just next to phase shift PWM, but PSC PWM has major disadvantage of highest THD. So, the TTMC SVPWM is the best choice for minimum THD and maximum output voltage.

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